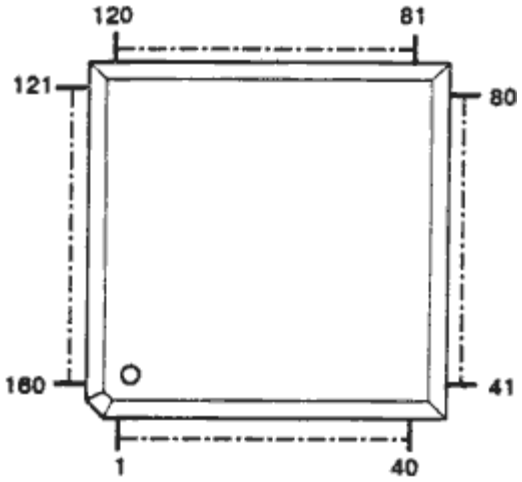
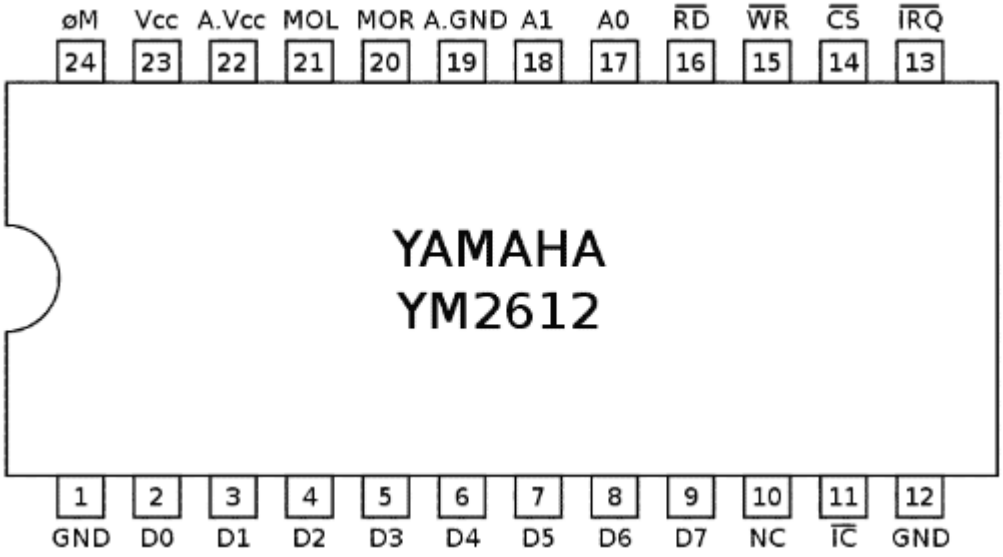
Sega IC CUSTOM CHIP UPD92271 315-5433



■ Pin Name

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	VDD	41	GND	81	VDD	121	GND
2	MCLK	42	GND	82	A07	122	GND
3	CART	43	ZA4	83	A08	123	VCLK
4	ZRMM	44	ZA3	84	A09	124	XM3
5	XREF	45	ZA2	85	A10	125	XAS
6	XM1	46	ZA1	86	A11	126	LDS
7	ZRSS	47	ZA0	87	A12	127	UDS
8	XZBR	48	QA4	88	A13	128	RW0
9	WAI	49	QA6	89	A14	129	DTK
10	ZBAK	50	QA0	90	A15	130	BG
11	ZWW	51	QA1	91	A16	131	BGA
12	ZRR	52	QA2	92	A17	132	BR
13	IREQ	53	QA3	93	A18	133	HALT
14	MRQ	54	QA5	94	A19	134	VRES
15	XNMI	55	QB4	95	A20	135	XVPA
16	ZD1	56	QB6	96	A21	136	FC0
17	ZD0	57	QB0	97	A22	137	FC1
18	ZD7	58	QB1	98	A23	138	D00
19	GND	59	QB2	99	GND	139	D01
20	VDD	60	QB3	100	VDD	140	D02
21	GND	61	QB5	101	HL	141	D03
22	ZCLK	62	QC0	102	XFDW	142	D04
23	WRES	63	QC1	103	XFDC	143	D05
24	ZD2	64	QC2	104	XDIS	144	D06
25	ZD6	65	QC3	105	FRES	145	D07
26	ZD5	66	QC4	106	VDPM	146	D08
27	ZD3	67	QC5	107	XROM	147	D09
28	ZD4	68	QC6	108	ASEL	148	D10
29	ZAF	69	TST0	109	XTIM	149	D11
30	ZAE	70	TST1	110	RAS2	150	D12
31	ZAD	71	TST2	111	CAS2	151	D13
32	ZAC	72	XJAP	112	XOE0	152	D14
33	ZAB	73	A01	113	CAS0	153	D15
34	ZAA	74	A02	114	SRES	154	NTS
35	ZA9	75	A03	115	XCE0	155	HSYC
36	ZA8	76	A04	116	XLWR	156	SOUN
37	ZA7	77	A05	117	IA14	157	INTA
38	ZA6	78	A06	118	XNOE	158	EDCK
39	ZA5	79	GND	119	XEOE	159	GND
40	VDD	80	GND	120	VDD	160	GND

Yamaha **YM2612 (OPN)** Sound Chip



No.	Pin Name	I/O	Function
1	GND	–	Ground pin.
2	D_0	I/O	8-bit bidirectional data bus. Communicates data with the processor.
3	D_1		
4	D_2		
5	D_3		
6	D_4		
7	D_5		
8	D_6		
9	D_7		
10	$\overline{TEST}$	I/O	Pin to test this LSI. Do not connect.
11	$\overline{IC}$	I	Initializes the internal register.
12	GND	–	Ground pin.
13	$\overline{IRQ}$	O	Interrupt signal issued from the two timers. When the time programmed into the timer has elapsed, this goes low. Output with open drain.
14	$\overline{CS}$	I	Control the D0 – D7 data bus.
15	$\overline{WR}$		
16	$\overline{RD}$		
17	A_0		
18	A_1		
19	A GND	–	Ground pin.
20	MOR	O	Two-channel analog outputs. These are output with a source follower.
21	MOL		
22	A V_{CC}	–	+5V power supply pins.
23			
24	ϕ M V_{CC}	I	Master clock input.

CS	RD	WR	A1	A0	Details
0	1	0	0	0	Writes register addresses of timers, etc.
					Writes register addresses of channels 1-3.
0	1	0	0	1	Writes register data of timers, etc.
					Writes register data of channels 1-3.
0	1	0	1	0	Writes register addresses of channels 4-6.
0	1	0	1	1	Writes register data of channels 4-6.
0	0	1	0	0	Reads statuses.
1	X	X	X	X	D0 – D7 are set to high-impedance.